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PTO/SB/08B (08-03)

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Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	09/760,331
(Use as many sheets as necessary)				Filing Date	January 13, 2001
				First Named Inventor	Masatoshi Ishikawa
				Art Unit	2625
				Examiner Name	Seyed H. Azarian
Sheet	1	of	2	Attorney Docket Number	
876564/0083					

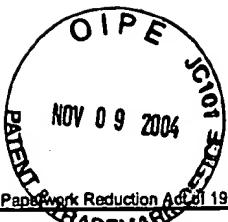
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Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.			T ²
S.A		"Moment Extraction Architecture for Digital Vision Chip", Technical Report of IEICE, July 1997 (citing the following 12 references).			
		C. Mead and M. Mahowald, "A Silicon Model of Early Visual Processing", Neutral Networks, July 1988.			
		M. Ishikawa, A. Morita, and N. Takayanagi, "High Speed Vision System Using Massively Parallel Processing", IROS, 1992.			
		Y. Nakabo, I. Ishii, and M. Ishikawa, "1ms Target Tracking System Using Ultra-Parallel Ultra-High Speed Vision", 1997.			
		T. Oowaki, Y. Nakabo, A. Namiki, I. Ishii, and M. Ishikawa, "Real Time System for Virtually Touching Objects...", 1998 (no english abstract available).			
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		I. Ishii, Y. Nakabo, and M. Ishikawa, "Target Tracking Algorithm for 1ms Visual Feedback System Using Massively Parallel Processing", IEEE, 1996.			
		T. Konuro, S. Suzuki, I. Ishii, and M. Ishikawa, "Design of Massively Parallel Vision Chip Using General-Purpose Processing Elements", 1998 (no english abstract available).			
		M. Ishikawa, K. Ogawa, T. Komuro, I. Ishii, "A CMOS Vision Chip with SIMD Processing Element Array for 1ms Image Processing", February 1999.			
↓		T. Bernard, B. Zavidovique, and F. Devos, "A Programmable Artificial Retina", IEEE Journal of Solid-State Circuits, July 1993.			

Examiner Signature	Seyed H. Azarian	Date Considered	6/20/05
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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S.A			
		J. Eklund, C. Svensson, and A. Astrom, "VLSI Implementation of a Focal Plane Image Processor...", IEEE Trans. VLSI Systems, September 1996.	
		T. Mukai and M. Ishikawa, "Two-Dimensional Coordinates Transform Circuit for Parallel Processing Vision", Technical Report of IEICE, 1992.	
		I. Ishii, T. Komuro, and M. Ishikawa, "Moment Calculation Method using Bit-Plane Feature Decomposition", Technical Report of IEICE, July 1999.	

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